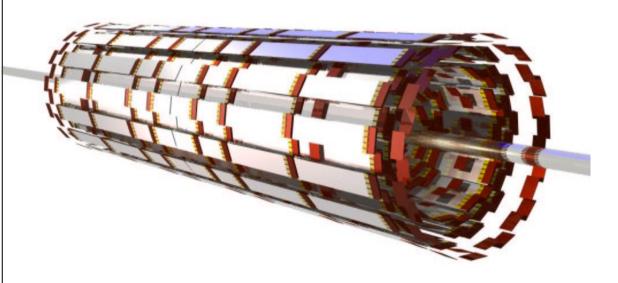


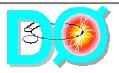
The Upgraded D0 Silicon Microstrip Tracker For Fermilab Run2b

Ron Sidwell, Kansas State University,
For the D0 collaboration





Why a new silicon detector?

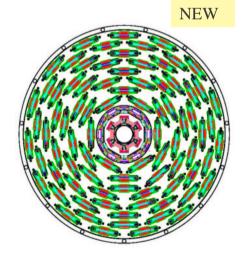


- Extended running at higher luminosity is now foreseen at Fermilab. The current detector was designed for 2 fb⁻¹, now plan 15 fb⁻¹ for Run IIb.
- Improved Higgs sensitivity- add inner layer, increase lever arm for better impact parameter measurement w.r.t current detector.

• FEATURES of new detector

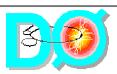
- <u>Keep it simple:</u> single-sided sensors, no pitch adapters, minimal number of parts types
- Complete replacement
- Barrels only, no disks- concentrate on high PT physics
- New SVX4 readout chip
- Target late 2005







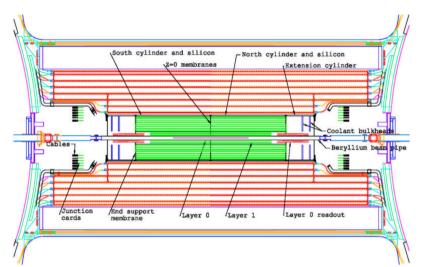
Detector Design



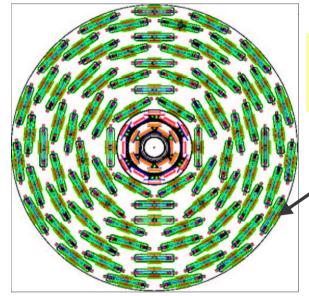
Section

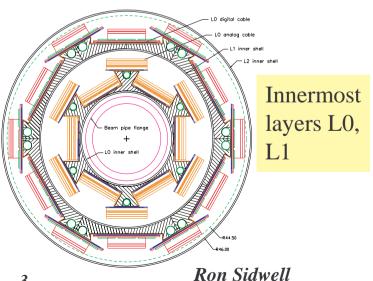
Stave

view.



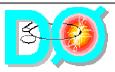
Plan view. Built in two sections, meet at z=0. Insert 6 silicon layers inside of central fiber tracker (18 planes of scintillating fiber).





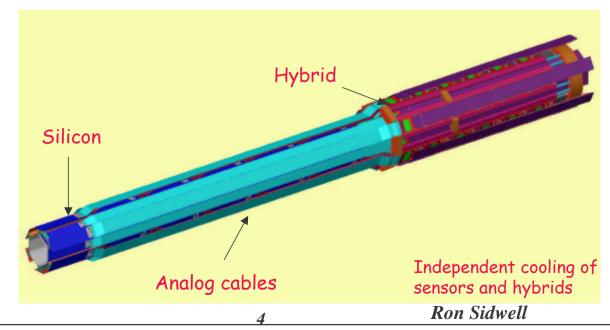


Layer 0 and Layer 1



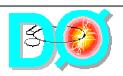
• Layer 0 and 1

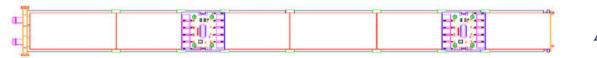
- Tight space, not supported by beam tube.
- Minimize material
- Cool to -10 °C to increase sensor lifetime
- No hybrids mounted on sensors for L0: analog cables



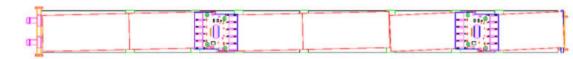


Staves (Layers 2-5)



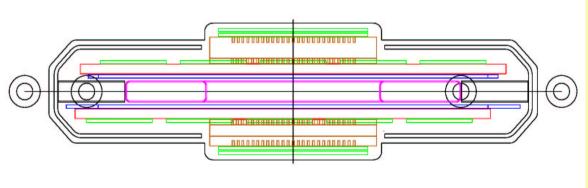


Axial



Stereo

Module configuration for outer layer staves. Stereo angle is 1.24 or 2.48 deg.

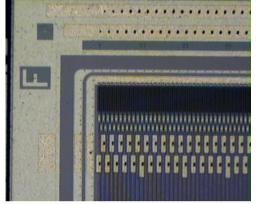


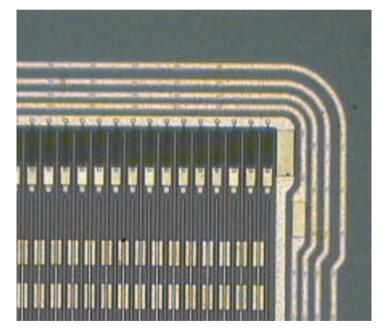
Stave Cross
Section (168
needed).
Supported in
bulkheads at
z=0, 605mm



Inner sensors



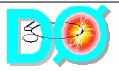


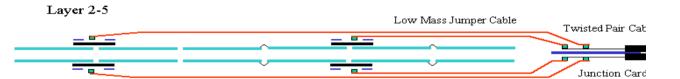


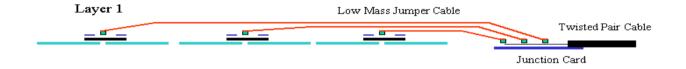
- Must be radiation-hard (up to 15 Mrad)
- Required: breakdown >700V, depletion < 300v.
- Pitch
 - 50 μm, L0
 - 58 μm, L1
- Photos: Detail of
 Hamamatsu (upper) and
 ELMA (lower) prototype
 sensors for the inner
 layers. Note the differing
 guard ring structure.

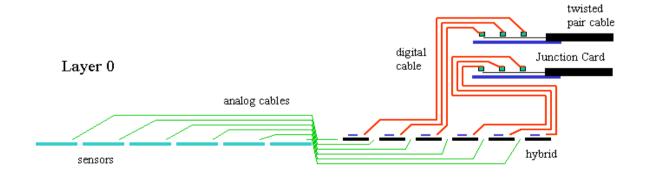


Front-end Readout Cables



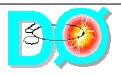






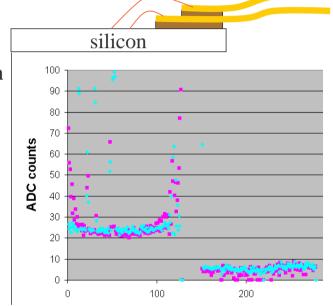


Analog Flex Cables



• For layer 0 need low mass, fine pitch, flex cables to carry analog signals to hybrids

- Technically stimulating
 - Trace width ~ 15 20 μ m, pitch 91 μ m
 - 2 cables offset by 50 μm
- Noise determined by capacitance
 - For S/N > 10: C < 0.55 pF/cm
 - current design, with 16mm trace width -> 0.32 pF/cm
- Prototype cables (Dyconex)
 - First batch: 10/12 cables good.
 - Two had 2 open/shorts
 - Second batch: 25/27 cables
 - Two with ≥ 2 open/short
 - Cables laminated and bonded
- Shielding needed -
 - Cable is antenna for RF

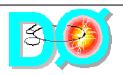


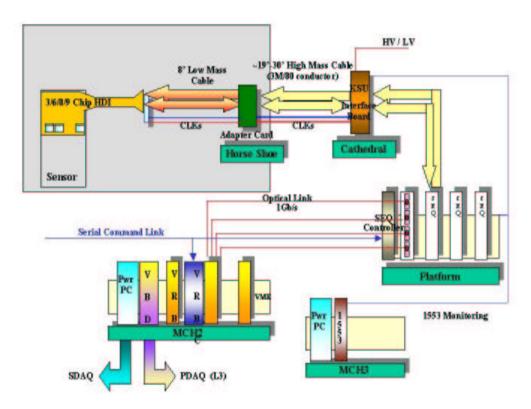


Ron Sidwell



Changes to readout

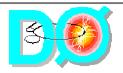


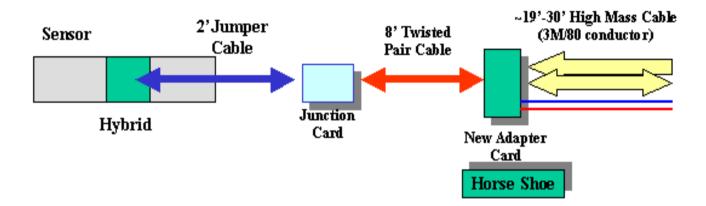


- Area in gray is replaced..
- Recycle most cables, and all downstream electronics.



New Front End

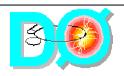


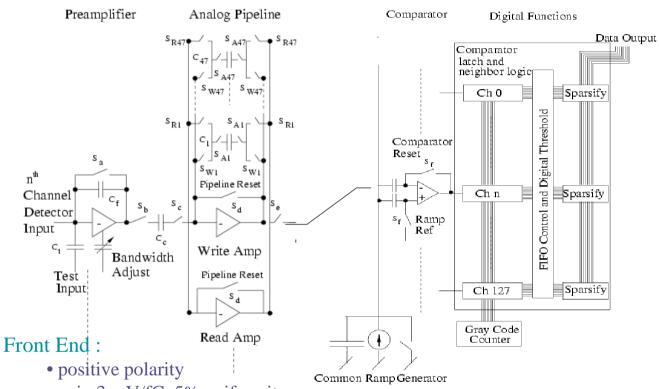


- Ceramic hybrid with new SVX4 readout ICs.
- Flex Jumper cable 50-100cm long.
- Passive Junction card solder twisted pair at one end
- Plug twisted pair plus clocks into active adapter card



SVX4 Chip





- gain 3 mV/fC, 5% uniformity
- load 10 40 pF
- risetime 60-100 nsec
- dynamic range 200 fC
- 'black hole' clumping
- reset time 200 nsec
- pipeline 42 cells

IEEE 11/02

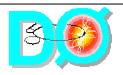
Back End:

- Wilkinson ADC, 106 MHz counter
- dynamic pedestal subtraction
- data sparsification
- neighbor logic
- differential output drivers upto 17 mA
- configuration register

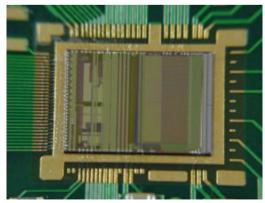
Ron Sidwell

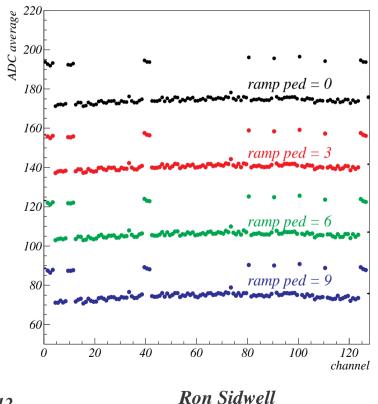


SVX4 chips



- Design effort began (11/00)
- Joint effort of Fermilab, LBL, Padua
- Prototypes delivered in 6/02
 - Works in DØ and CDF modes
 - Known fixes, more tests to do
 - 2nd proto submission 1/03
- DØ involved early in testing. Main problem to fix is non-uniform pedestal.

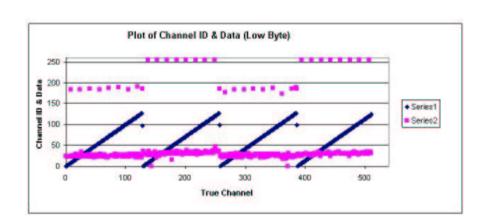


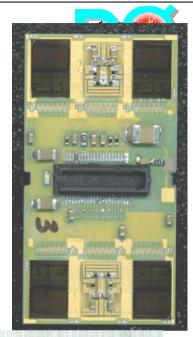


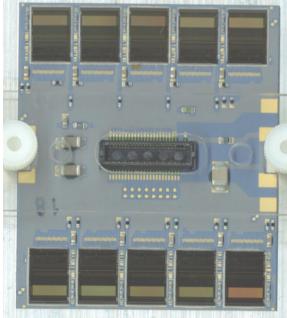


Hybrids

- Double ended readout
- Prototypes exist and work for L1 and L2-3
- Important to work with vendors from the start (CPT, Amitron)
- Commercial stuffing

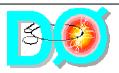


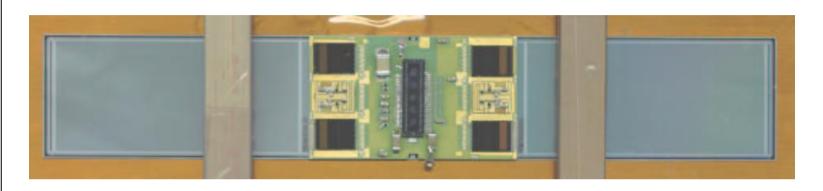


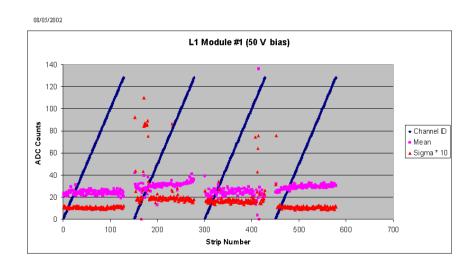




Prototype L1 Module







- Two L1 ELMA sensors
- L1 prototype hybrid (stuff 4/6 SVX4 chips)
- It works!



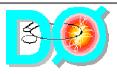
Conclusion



- Simulations show new design increases Higgs efficiency ~40% relative to current setup. More luminosity buys x7.
- Design, prototyping, and costing are in good shape. Reviews have been very positive.
- Waiting DOE final approval in Dec '02.
- Aggressive schedule aims for late '05 installation.



Contributions



- Sensor Testing
 - Kansas State, SUNY StonyBrook, CINVESTAV, Moscow State
- Readout Electronics
 - FNAL, Kansas State, Kansas, UIC, Fresno State, Brown, Louisiana Tech, Northwestern, Zurich
- Mechanical Design and Fabrication
 - FNAL, Washington, Michigan State
- Monitoring
 - NIKHEF, Rice
- Funding: 131 FTE-years; cost ~\$13M + conting.;
 DOE + NSF MRI